

# Main Memory Unit

## Final Report

(NASA-CR-120733) MAIN MEMORY UNIT Final Report, Oct. 1973 - Apr. 1975 (International Business Machines Corp.) 31 p HC \$3.75

N75-21981

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## 1.0 INTRODUCTION

This report describes the work completed by IBM on contract NAS8-30460. The period of performance for this work was from October 1973 to April 1975. The work was divided into two phases which resulted in the development of a Main Memory Unit (MMU) for the Space Ultrareliable Module Computer (SUMC) Model HTC.

Phase I was for the design, fabrication and test of Basic Memory Modules (BMM) which were to be used in the design and construction of the MMU. The BMM was designed from state-of-the-art technologies which included Large Scale Integration (LSI) devices mounted and interconnected on a substrate to form a functional module to be utilized in the MMU development.

Phase I also included a SUMC memory system design study. This study addressed itself to the BMM design and analysis to be conducted to determine the most efficient organization of the BMM in order to establish such modularity features as; word length expandability without redesign; high reliability; and fault tolerance.

Phase II was to design, fabricate, test and deliver one MMU which will be electrical and mechanically compatible with the Hybrid Technology Computer (HTC) model of the SUMC family of computers. The MMU will contain a storage capacity of 8196 36 bit words which includes a parity bit for each 8 bit byte of data.

## 2.0 SUMMARY AND CONCLUSIONS

### 2.1 Basic Memory Module

This section describes the construction and electrical characterization of the 4086 x 2-bit Basic Memory Module (BMM) designed and fabricated by IBM under Contract NAS8-30460. This module was developed for the Space Ultra-reliable Modular Computer (SUMC) program.

The module uses four 2K x 1-bit N-channel FET, random-access memory (RAM) chips, called "array chips", and two sense amplifier chips, mounted and interconnected on a ceramic substrate. Figure 2-1 shows the module with its ceramic cover removed.

Four 5% tolerance power supplies are required. At the module, the address, chip select, and array select lines require a 0-8.5 V MOS signal level. The data output, read-strobe, and write-enable lines operate at TTL levels.

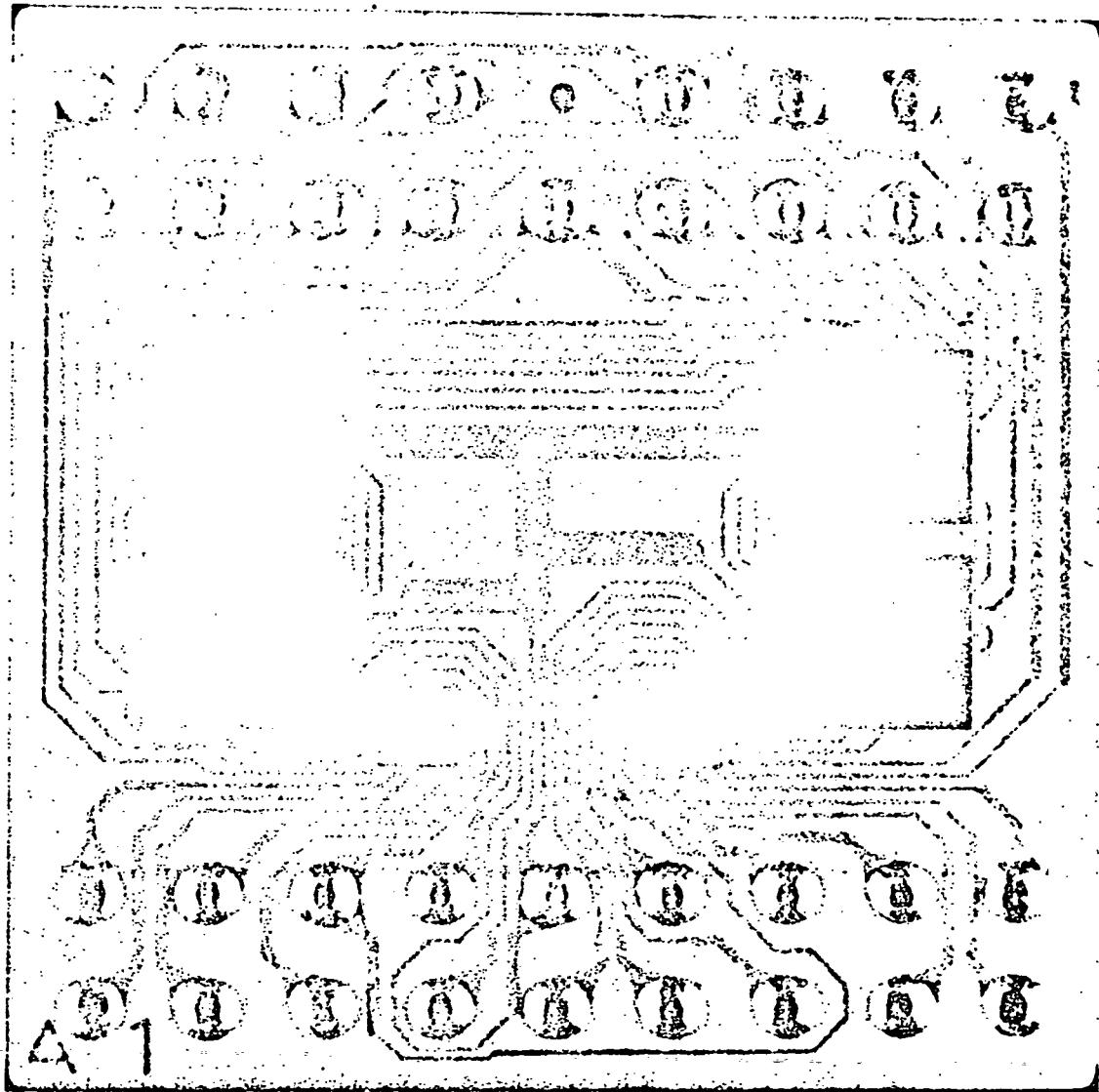
Although the module is organized as 4096 x 2 bits, it can be used in a 8196 x 1-bit application with appropriate external connections, as shown in Figure 2-2. A 4096 x 1-bit organization can be obtained by depopulating chips.

Originally, only one dual sense-amplifier chip was planned, with each amplifier servicing a single output bit. It was subsequently determined that the dual sense amplifier chip of interest had on-chip wiring in the output stage that precluded the 8196 x 1-bit organization. Thus, it was necessary to use two of these sense amplifier chips with only one of the dual amplifiers actually connected and powered on each chip. This was the only change from the originally proposed BMM.

Table 2-1 summarizes the most important measured performance characteristics of the device for selected conditions. Only room temperature functional testing was required, but a rather comprehensive electrical characterization was actually performed. The results are presented in the Basic Memory Module final report, IBM report number 74-585-006.

The memory and sense amplifier chips are standard IBM commercial devices, and the ceramic substrate and interconnection techniques are standard IBM commercial technology. Inherently then, the BMM has the advantages of a large chip production base, low cost, and an immense amount of relevant field experience to support its projection of high reliability.

Detailed information on the BMM is available in the Basic Memory Module final report delivered under NAS8-30460 (IBM Report Number 74-585-006).



(Flecks showing on the substrate are epoxy residue after cover removal)

Figure 2-1. BMM Substrate and Chip Layout

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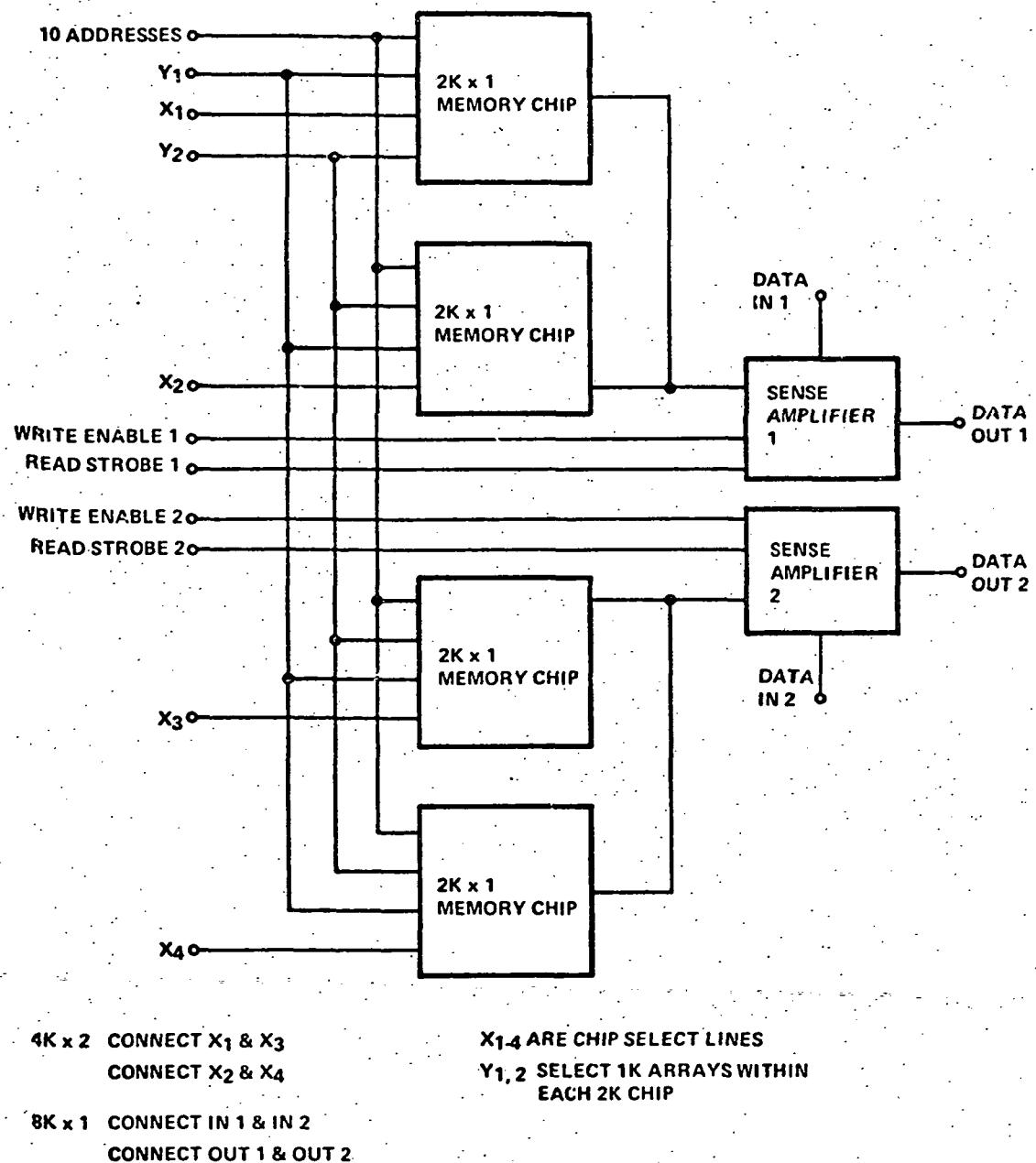


Figure 2-2. Basic Memory Module Block Diagram

Table 2-1  
SUMMARY OF IMPORTANT MEASURED BMM CHARACTERISTICS

Parameter	Test Conditions	Parameter Value
Read Access Time From Chip Select ( $T_{AX}$ )	+35°C, not-strobed, nominal supply voltages +125°C, not-strobed, worst-case voltages -47°C, not-strobed, worst-case voltages +125°C, strobed, worst- case voltages	111.7* ns 166.6* ns 98.5* ns 108.6* ns
Read Access Time From Address ( $T_{AA}$ )	As above	0 to 10 ns greater than $T_{AX}$
Minimum Write Pulse Width	Worst-case temperature and voltage	$\leq$ 25 ns
Operating Power	+35°C, 250 ns cycle, nominal voltage      { 4K x 2 8K x 1 +125°C, 250 ns cycle,      4K x 2 worst-case voltage	635* mW 466* mW 617* mW
Standby Power	+35°C, 250 ns cycle,      4K x 2 nominal voltages	297* mW
Capacitance Chip Select Line Array Select Line All Others	+35°C	$\leq$ 66 pF $\leq$ 30 pF $\leq$ 22 pF
<p>*Average Value **Extrapolated Value All Temperatures are Case Temperatures.</p>		

## 2.2 SUMC Memory System Design Study

The purpose of this study was to examine memory organization options and recommend a preferred implementation in terms of partitioning and fault-tolerant hardware utilizing the SUMC basic memory modules (BMM's) being developed by MSFC under Contract NAS8-30460. To this end, certain assumptions were ground ruled, several alternatives within these ground rules examined, and conclusions were reached relative to a preferred implementation.

The major ground rule assumptions are:

1. Those aspects of the design with relatively high non-recurring costs should be applicable (without significant modification) to a diversity of applications.
2. There should be the maximum reasonable commonality with non-fault tolerant SUMC memory systems -- e.g., interface compatibility.
3. There should be a minimum of performance penalty from the fault-tolerant implementation.
4. The selected implementation should be amenable to extension to tolerate multiple array faults by utilization of spare units.

In this study a fault-tolerant memory is a storage system which can tolerate any (or virtually any) single component failure without producing erroneous results. This is achieved by implementing appropriate redundancy throughout the memory system. Failures in the random access storage element array are circumvented by storing words encoded in an error correction code (ECC) which may be used to detect and correct erroneous bits in words read from the memory, provided they are confined to a single memory module source. Failures outside the array are handled by other means.

A translator is interposed in the data flow path between the memory system and the units which communicate with memory. The translator performs several functions. The translation function involves translating byte parity encoded words received from external devices to a word encoded in an error correction code (ECC). The inverse translation is performed on read operations. The translator also performs checking to detect errors on all encoded information, and signals in the event it detects a discrepancy. On fetch operations the translator may in some cases be able to circumvent certain error conditions if they fall within the class correctable by the ECC.

The basic memory modules being developed by NASA on this contract (NAS8-30460), are assumed for the storage elements. These can be utilized without internal module alteration as  $8K \times 1$  bit modules as depicted in Figure 2-3, or alternatively as  $4K \times 2$  bit modules (where  $K = 1024$ ) as depicted in Figure 2-4. Only wiring differences external to the module determine which configuration is being utilized.

A thirty-two data bit memory is assumed. It is believed that this word length is an appropriate choice for SUMC applications. It is amenable to 16 bit wide data flow applications (e.g., the HTC has a 32 data bit memory word length with a 16 bit wide data flow in the CPU) as well as to 32 data bit wide data flow applications. The check bit overhead penalty incurred from error encoding is relatively less for a 32 bit word than for a 16 bit word. For a given storage capacity of data bits the storage efficiency (data bits (data + check bits)) is better for larger words, 64 bit words are more efficient than 32 which are more efficient than 16, etc. Translator hardware is somewhat greater for larger words so the design is a compromise as a function of word size (32 bits is a good compromise).

Two error codes were examined -- one a modified Hamming code which requires seven check bits to be stored with each 32 data bit word; the second a b-adjacent code with  $b = 2$ , which requires ten check bits to be stored with each word. Thus, the Hamming code requires only 70% as much storage overhead to implement. Additionally, the complexity of the Hamming translator is correspondingly less than for the b-adjacent. For these reasons as well as the fact that Hamming code translators have been widely used in commercial equipment (e.g., IBM System/370's) and well analyzed, it was decided to do a reasonably detailed functional logic design of the Hamming code translator for this study, b-adjacent codes are most appropriate when it is inconvenient and/or costly to organize the array in single bit wide independent slices. Magnetic technologies are a typical example of a technology where it is costly in terms of bit drivers to have single bit wide independent slices. With b-adjacent codes the slice may be several bits wide. Codes have been devised for  $b = 2, 4, 5, 8$ , and 16 to the author's knowledge.

Detail information on the above study is available in the report submitted under NAS8-3046, "SUMC Memory System Design Study", 15 March 1974, IBM, Huntsville, Alabama.

### 2.3 Main Memory Unit

The Main Memory Unit (MMU) represents an 8K memory slice which is compatible with the Hybrid Technology Computer (HTC) model of the SUMC family of computers. The MMU uses as its storage elements the Basic Memory Modules (BMM) developed under contract NAS8-30460. The MMU is organized such that

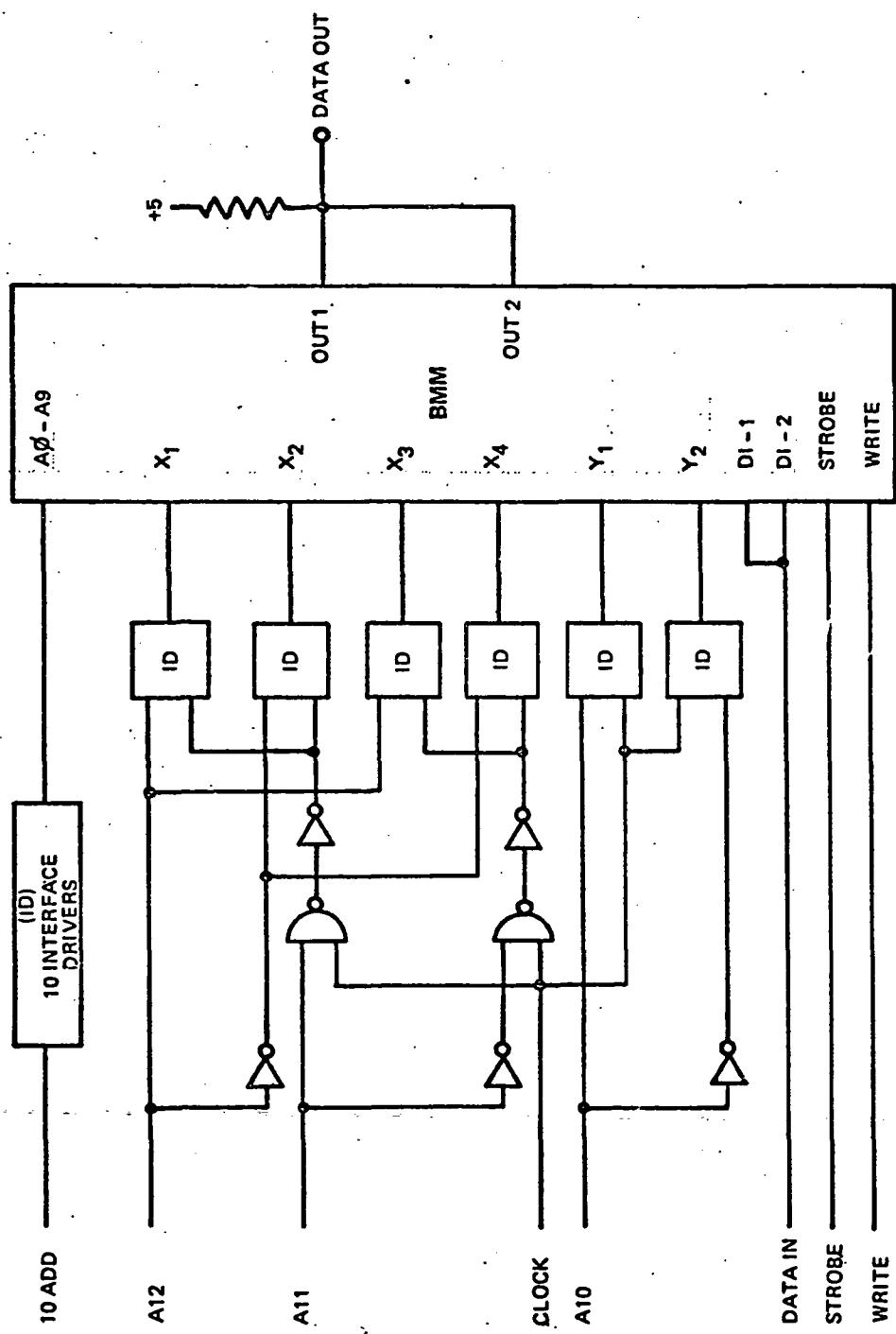


Figure 2-3. 8K x 1 Application BMM

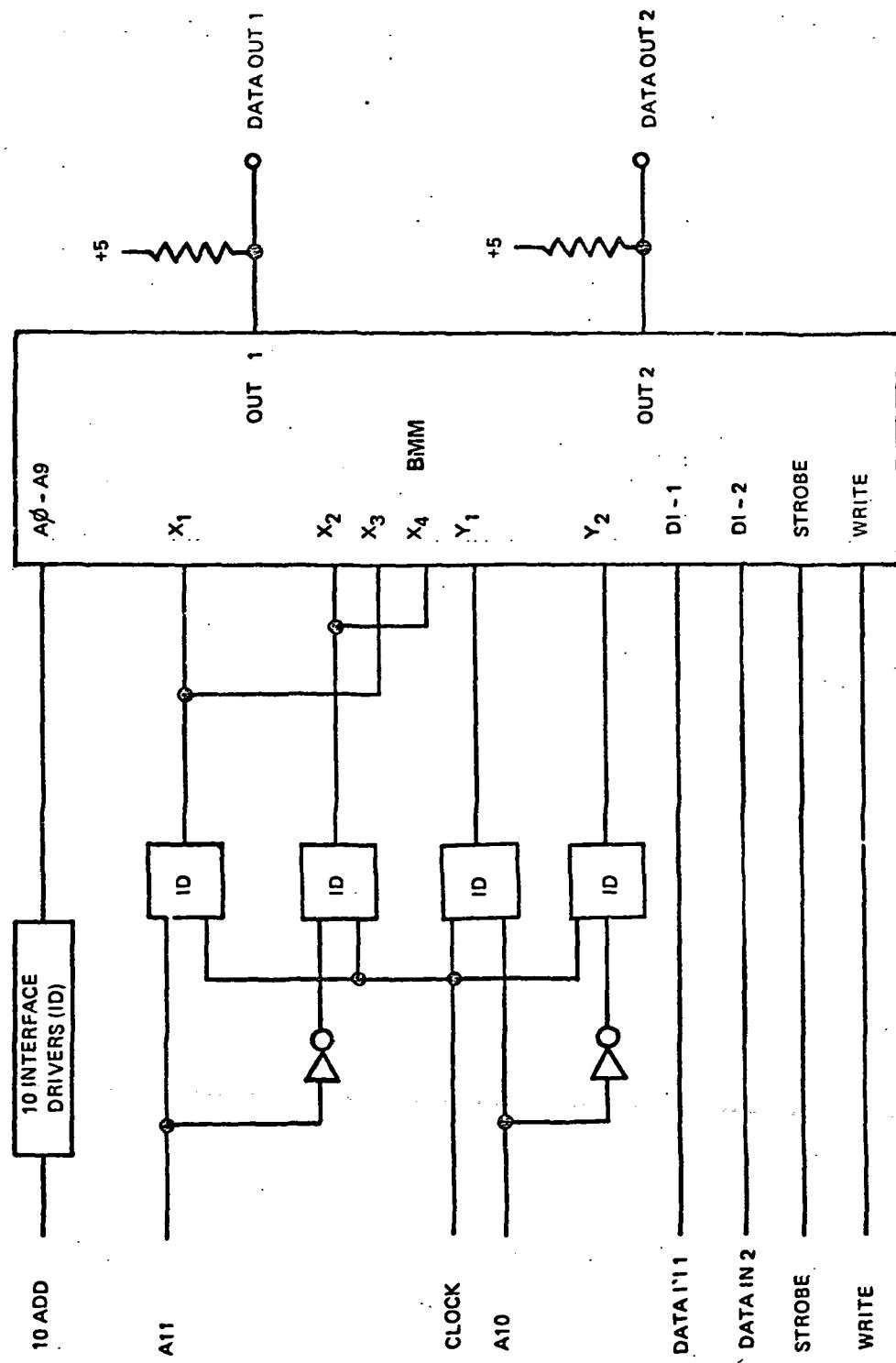


Figure 2-4. 4K x 2 Application BMM

two independent subassemblies, each capable of containing 4096 words of 36 bits, can be contained in one half of a single slice of memory. This organization provides modular capability for memory expansion in 4K by 36 bit increments. Furthermore, the MMU is designed such that multiple slices of the MMU can be interconnected to provide modular expansion of a main memory without additional electrical or mechanical redesign to the HTC.

The MMU has been integrated with the HTC and successfully passed memory diagnostic test when operating in conjunction with the HTC.

The following paragraphs in this report describe the MMU and its capabilities.

### 3.0 TECHNICAL APPROACH

The Main Memory Unit (MMU) is a 32K byte memory slice which is compatible with the Hybrid Technology Computer (HTC) model of the SUMC family of computers. The MMU uses the Basic Memory Modules (BMM) developed under contract NAS8-30460 as its storage elements. The MMU is organized such that two independent subassemblies, each containing 16,384 bytes (8 bits plus parity), can be contained in a single slice of memory. This organization permits modular capability for memory expansion in 16K byte increments. Furthermore, the MMU is designed such that multiple slices of the MMU can be interconnected to provide modular expansion of a main memory without electrical or mechanical redesign.

This is consistent with the SUMC philosophy which is that the storage units should be modular for easy expansion with maximum hardware efficiency and that only the items dependent upon the storage technology should be packaged with the storage elements. Parity checking and generating, storage protection and any architecture dependent error checking are performed in the CPU slice rather than in the storage slice for the reasons stated above.

#### 3.1 Electrical Design Considerations

The MMU is designed with a modularity of 16K bytes which are addressable on halfword (2 byte) boundaries per page (one half slice = one page). Each page is represented by Figure 3.1. The storage page contains 12 bit address decoding (10 on-chip and 2 off-chip), level shifting interface drivers, timing and control logic, data input buffers, output buffer registers, 18 BMMs, byte encoding logic, and a power regulator.

The data flow per storage page is 18 bits wide with the byte enable lines being encoded such that bytes 1 & 2 will be contained in the even addresses with bytes 3 & 4 in the adjacent odd address. This configuration establishes the modularity as 16K bytes of byte-addressable memory which is compatible with a 16 bit HTC. This configuration is diagrammed in Figure 3.2 which shows a 32K byte memory slice (two storage pages) configured for a 16 bit CPU. The data paths entering and leaving the storage slice are 36 bits (4 bytes) wide but are "dotted" into 18 bit busses at the CPU interface. Storage page A contains bits 0-17 while page B contains bits 18-35 with the page select lines from the CPU being used to determine which data will be gated onto the bus.

Figure 3.3 represents the 32K byte memory slice configured as an 8K fullword addressable memory. The control changes are shown in the figure and consist of separating the byte enable lines so they function on a full-word basis and using the page select lines to determine whether odd or even addresses are to be read. Both storage pages are exercised whenever either page select is activated and a 36 bit word can be read from memory. This technique allows the memory to be reconfigured with a minimum impact on the hardware.

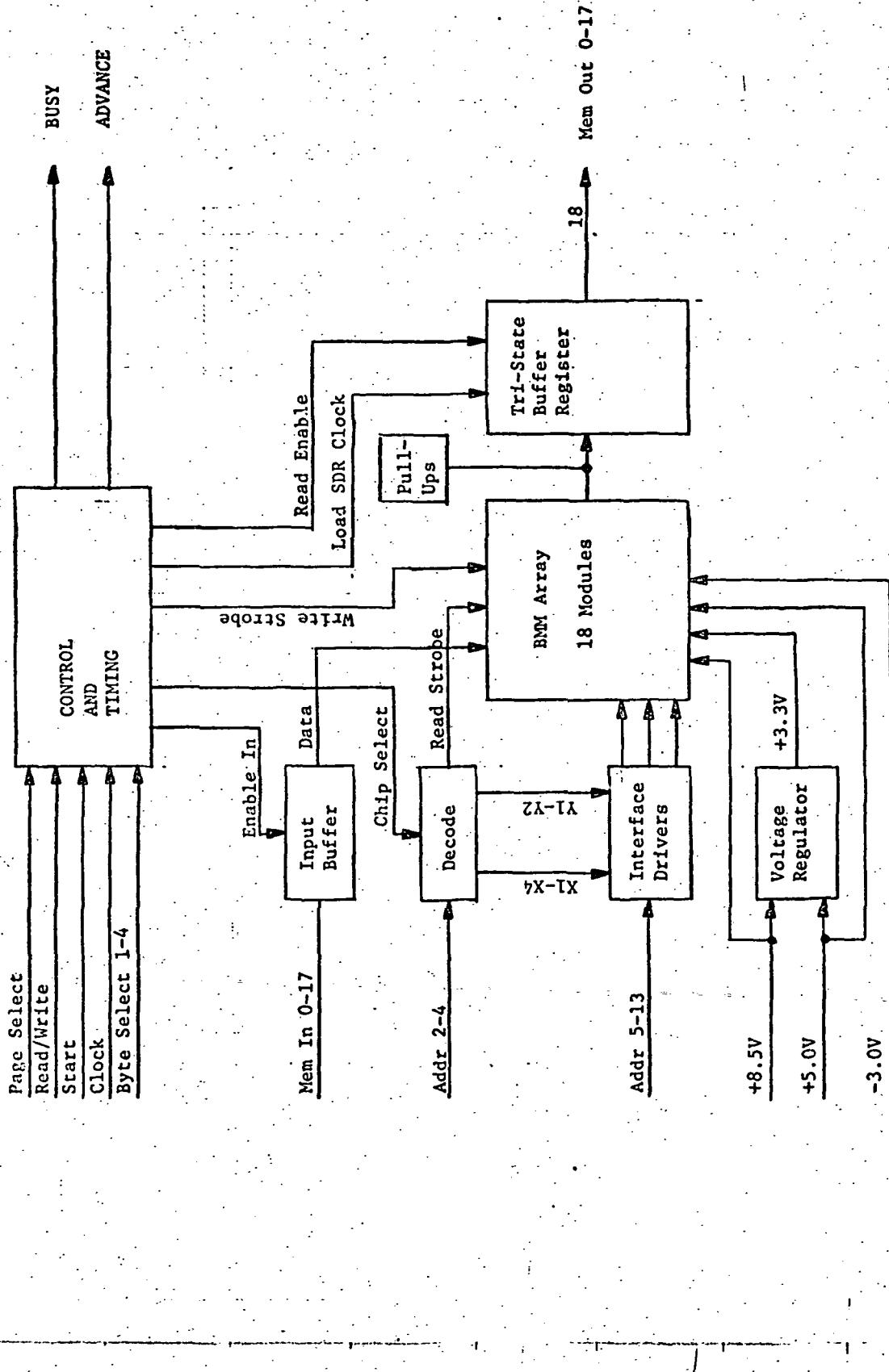


Figure 3-1. Main Memory Unit - Storage Page Block Diagram

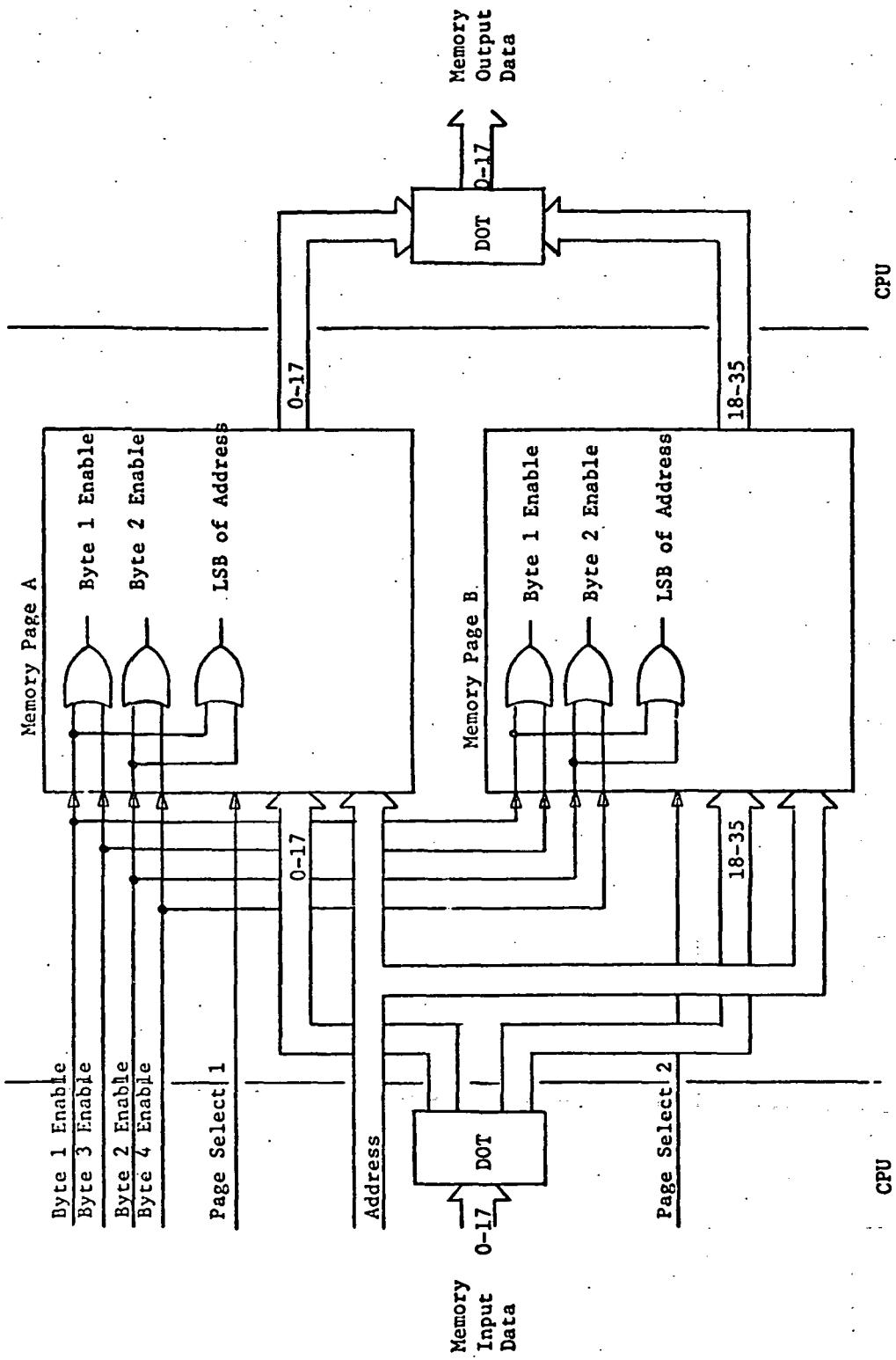


Figure 3-2. Main Memory Unit Configured for 16 Bit CPU

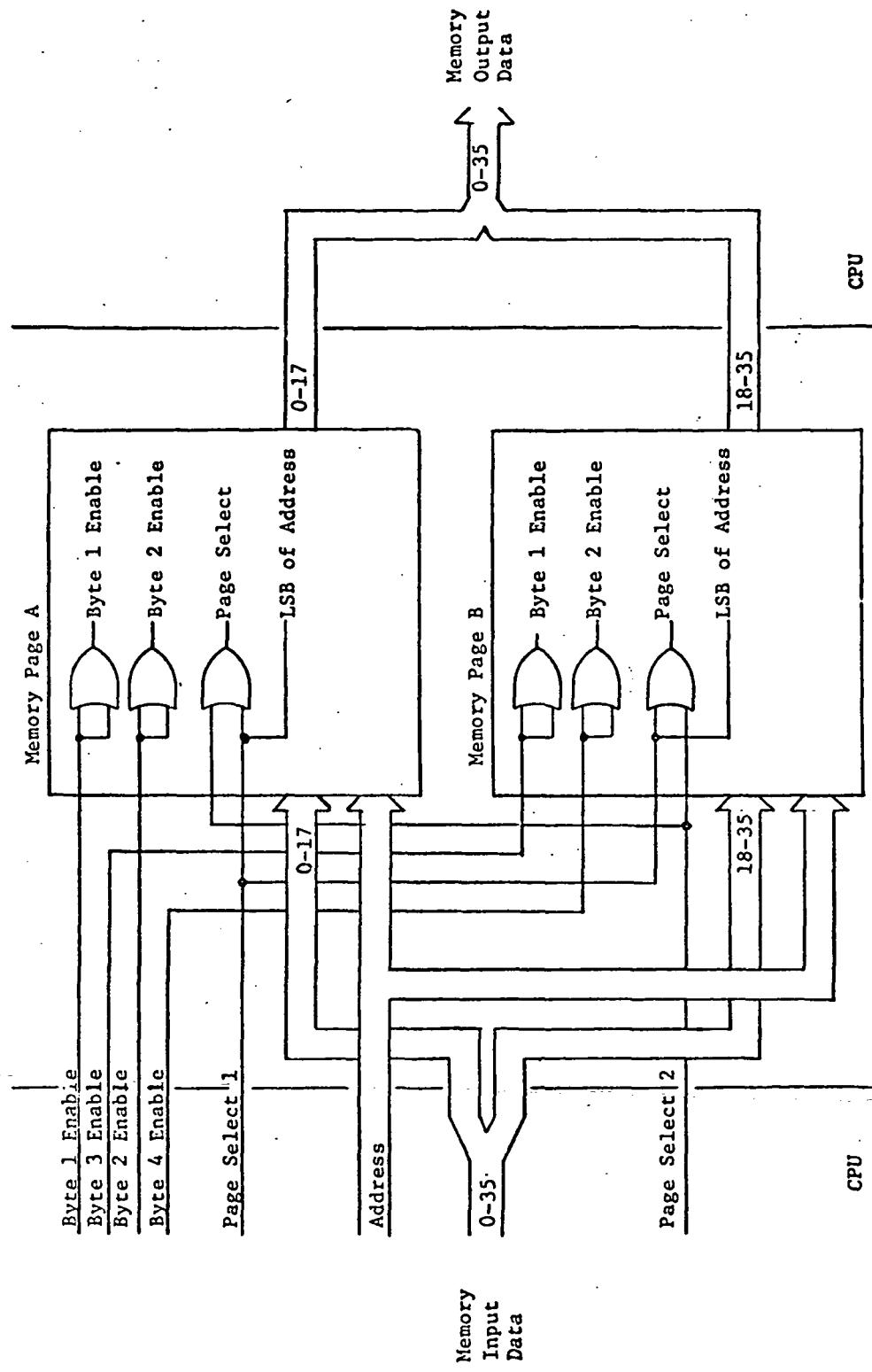


Figure 3-3. Main Memory Unit Configured for 32 Bit CPU

### 3.2 Main Memory Unit Mechanical Design

The MMU package is designed for use as a SUMC Modular Memory Slice. The SUMC Main Memory Unit (MMU) is a modular memory slice made up of a flexible/multilayer interconnection board (flex/MIB), a MIB and a main frame as illustrated in Figure 3-4. A part of the flex/MIB and MIB is a 40 mil thick copper heat frame bonded to the component mounting side. Components which interconnect with the MIB via soldered connections and plated thru holes are mounted with their bottom surfaces in contact with the heat frame. This same heat frame is in contact with the center web of the main frame when the populated MIBs are attached. The thermal path is completed thru the main frame to the external mounting feet. The dimensions of the memory slice are 10.7 in. long x 5.3 in. high x 1.4 in. thick not including the mounting feet.

One of the two interconnection boards of a slice, described as a flex/MIB, has a layer of flexible printed wiring cable laminated as an integral part of the MIB bonding process. This flexible cable extends beyond the non-flexible profile of the interconnection board and connects 120 circuits between the memory interconnection board assemblies mounted on each side of the main frame. The circuit connections are made thru a pluggable interface using a Burndy type ML-120 plug and receptacle.

The other interconnection board is a MIB containing a similar pluggable interface used to connect up to 240 circuits between slices by way of two flexible cables. One flexible cable is used primarily for a voltage/ground bus while the other contains up to 120 circuits. The flexible length of cable allows the disassembly of two adjoining slices for maintenance without need for circuit disconnect. An additional function of this interface is to provide memory expansion by interconnection of slices.

A single side of a memory slice will contain 4096 x 36 bit data words made up of the BMM pinned modules, power regulator, and support circuitry.

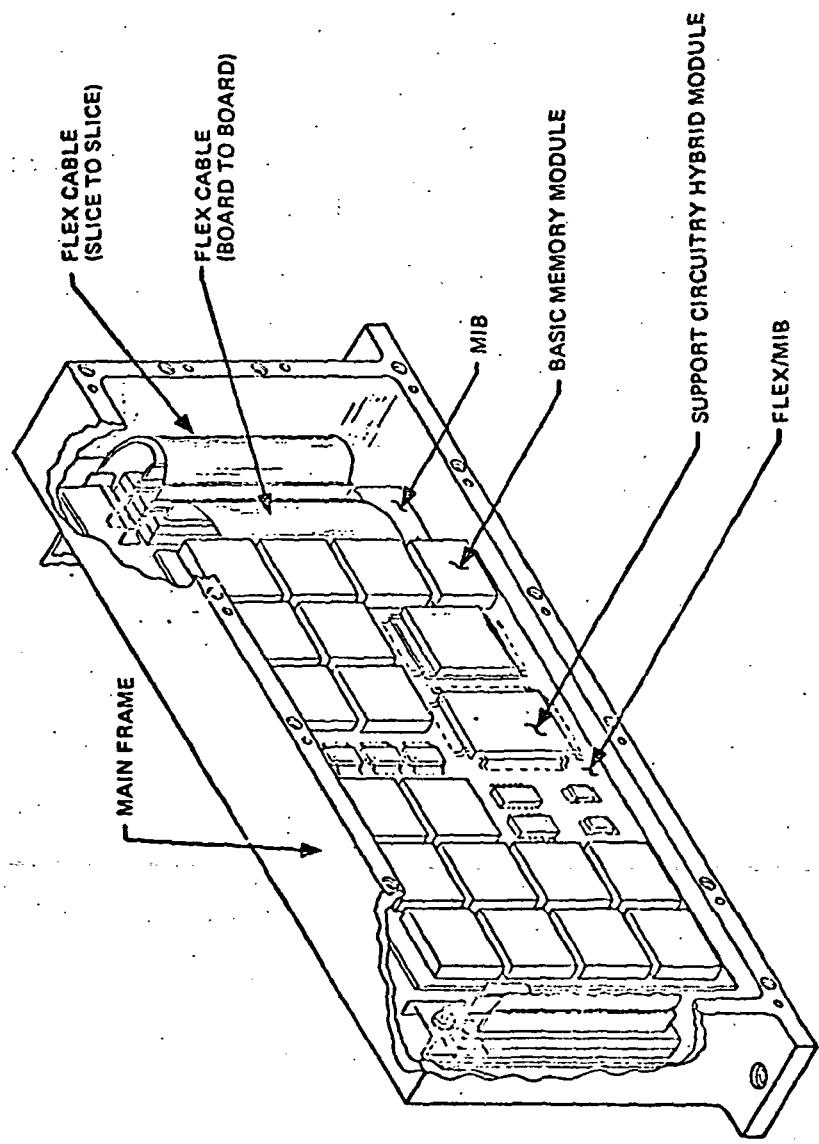


Figure 3-4. Main Memory Unit

#### 4.0 TEST RESULTS

The memory slice was integrated with the HTC model of the SUMC computer family and exercised with the diagnostic programs written for the HTC. The memory successfully passed all diagnostic routines.

The memory was designed to run at a higher speed than the present storage page and timing measurements verified this. The present memory operated with a memory cycle time of 770 nanoseconds while the new MMU has a cycle time of 520 nanoseconds. These cycle times are measured from the fall of the start signal to the fall of the memory busy signal. Figure 4.1 is a timing chart of the pertinent signals on the memory interface and internal to the storage page.

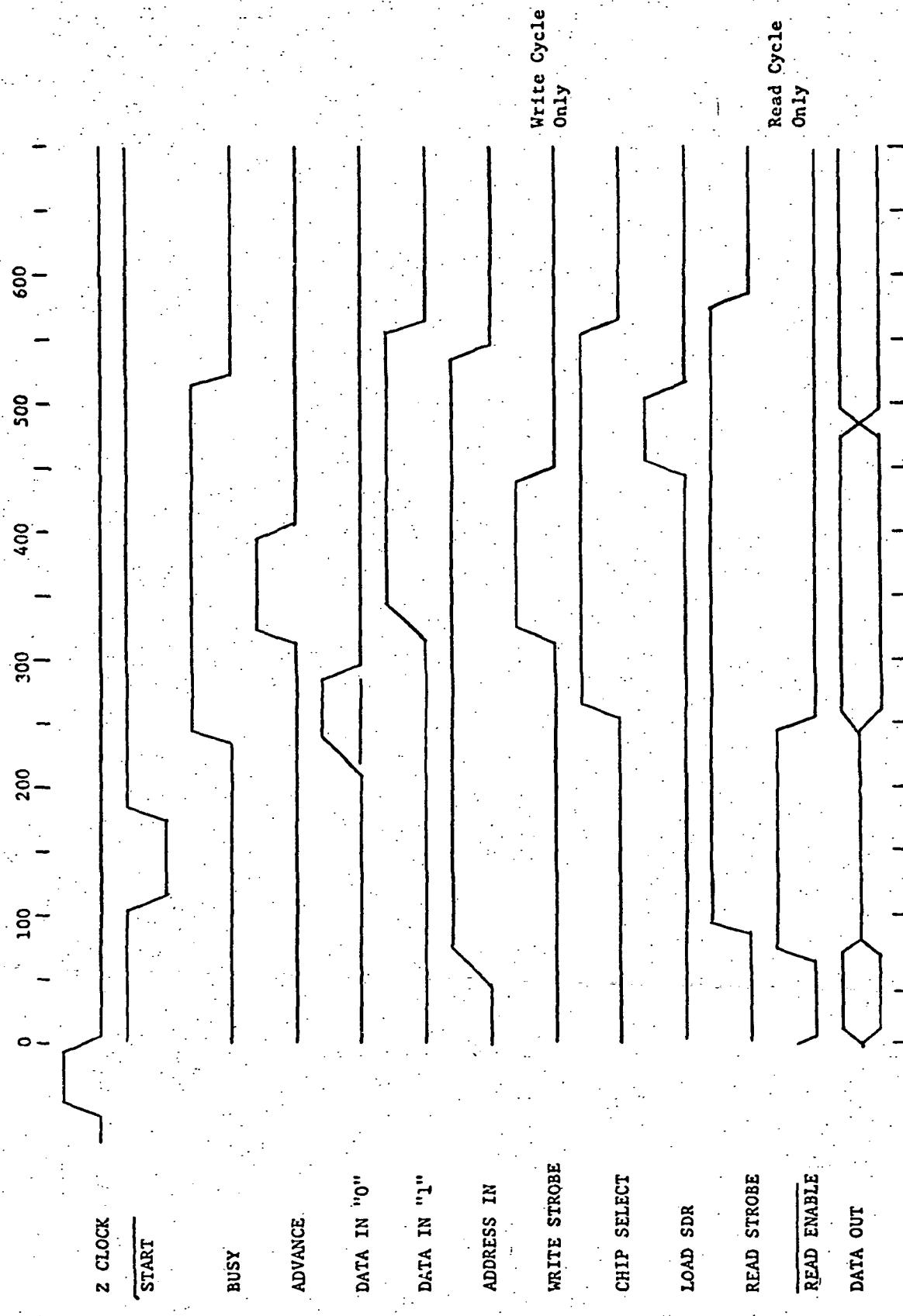
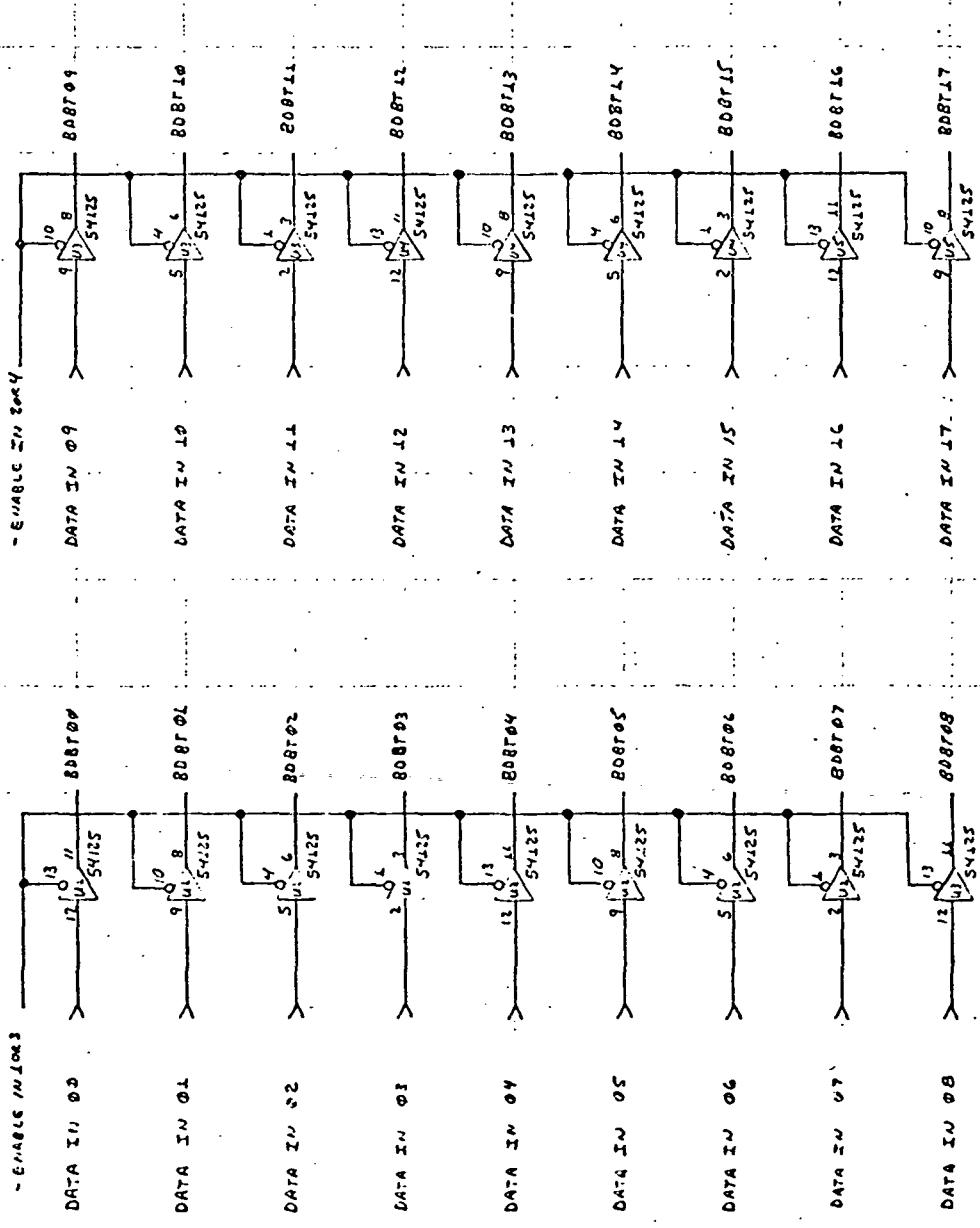


Figure 4-1. Main Memory Unit - Read/Write Timing

## 5.0 DOCUMENTATION

The documentation contained in this section is not intended to be a complete set but contains logic drawings to aid in understanding the design of the Main Memory Unit. The net lists applicable to the storage pages are NL7930350 and NL7930360 for storage pages A and B respectively.

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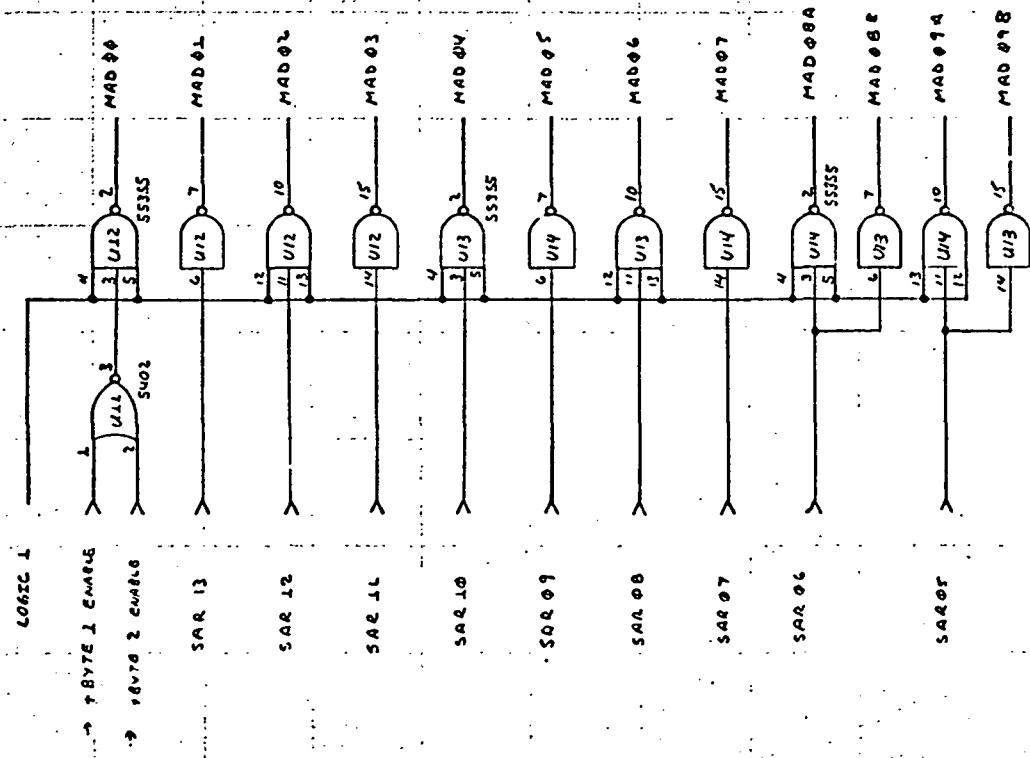


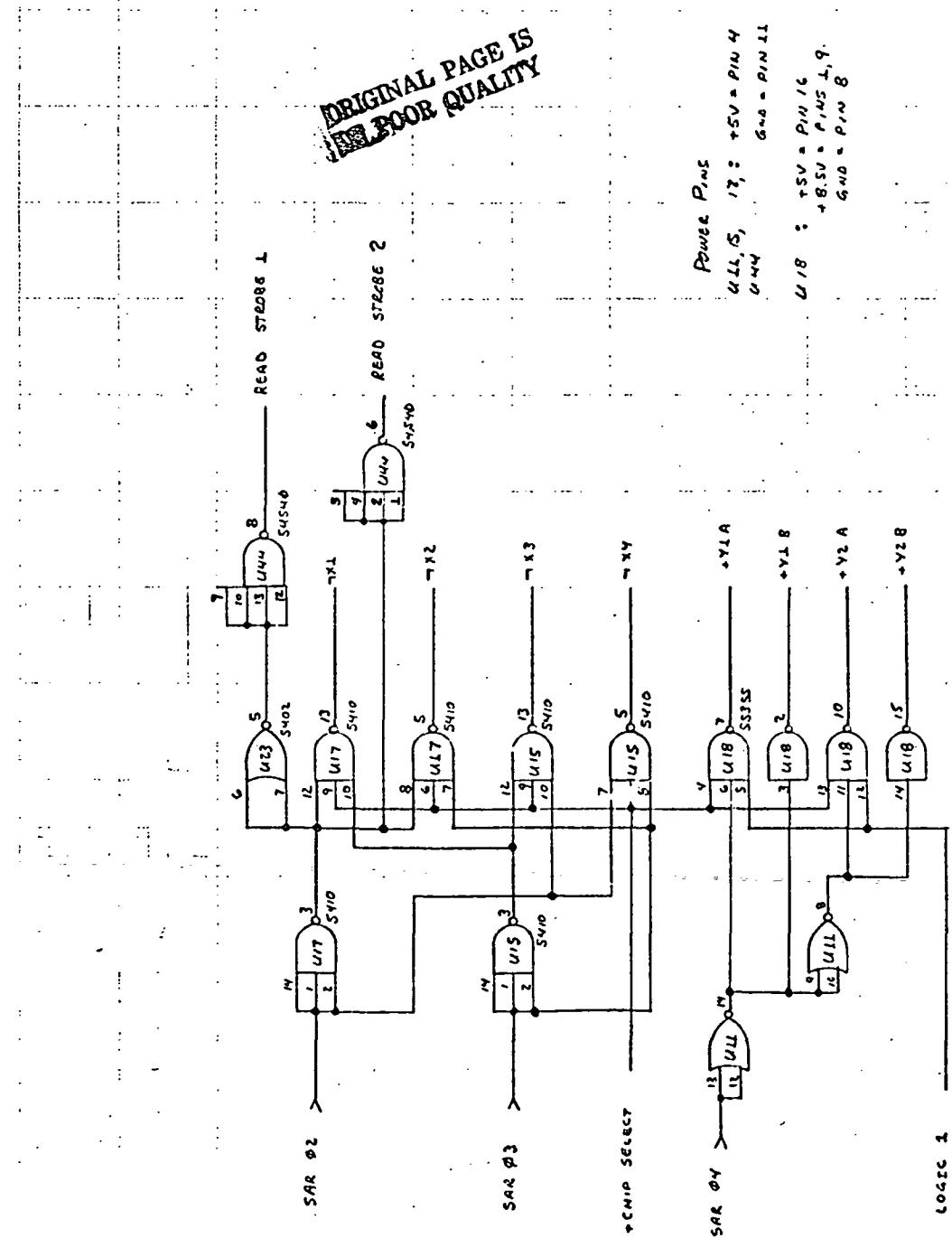
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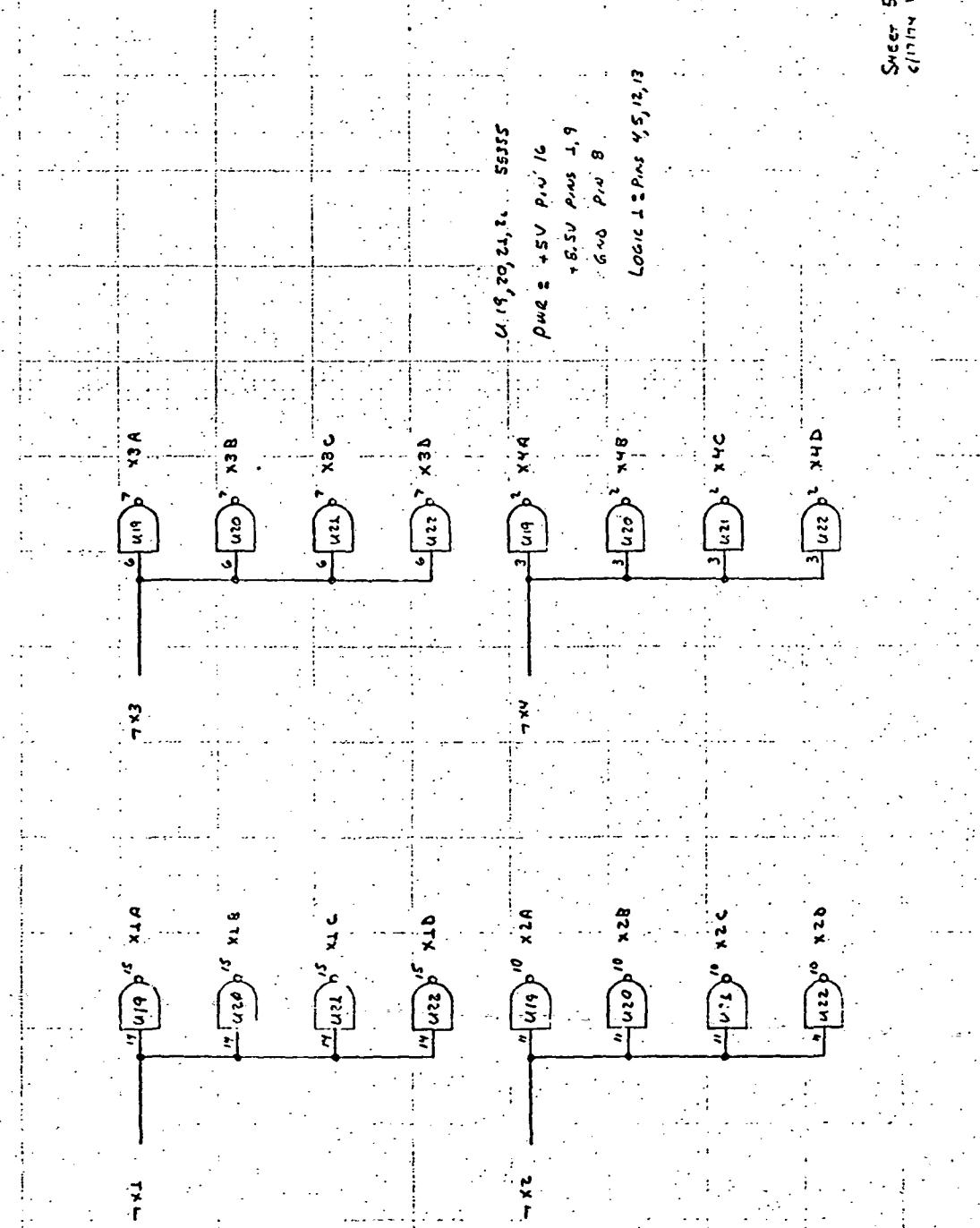
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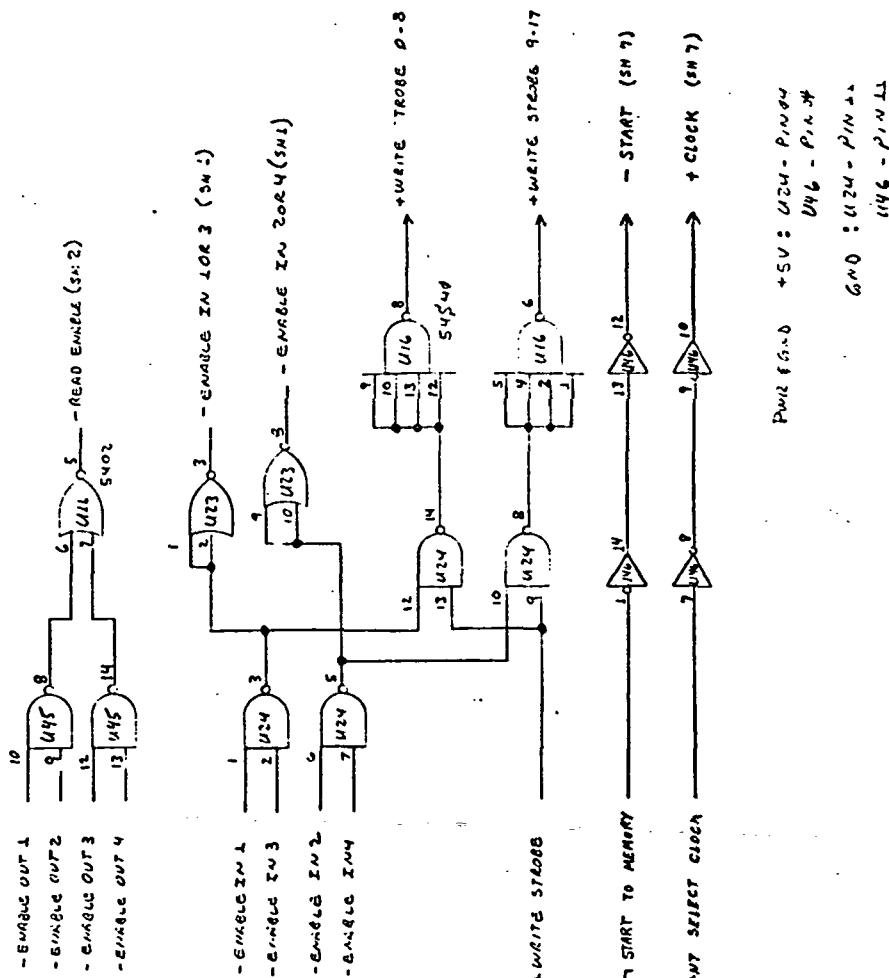




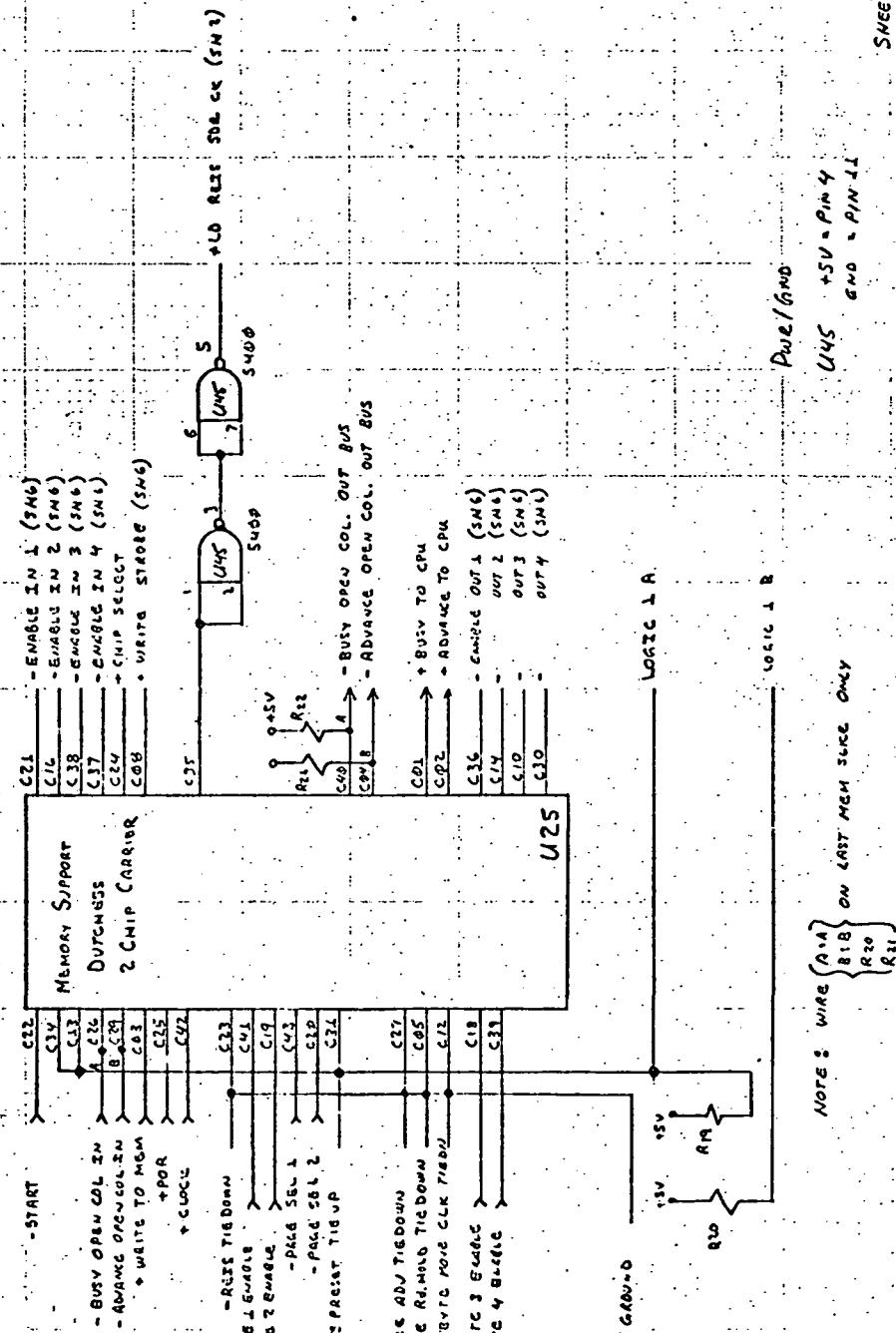


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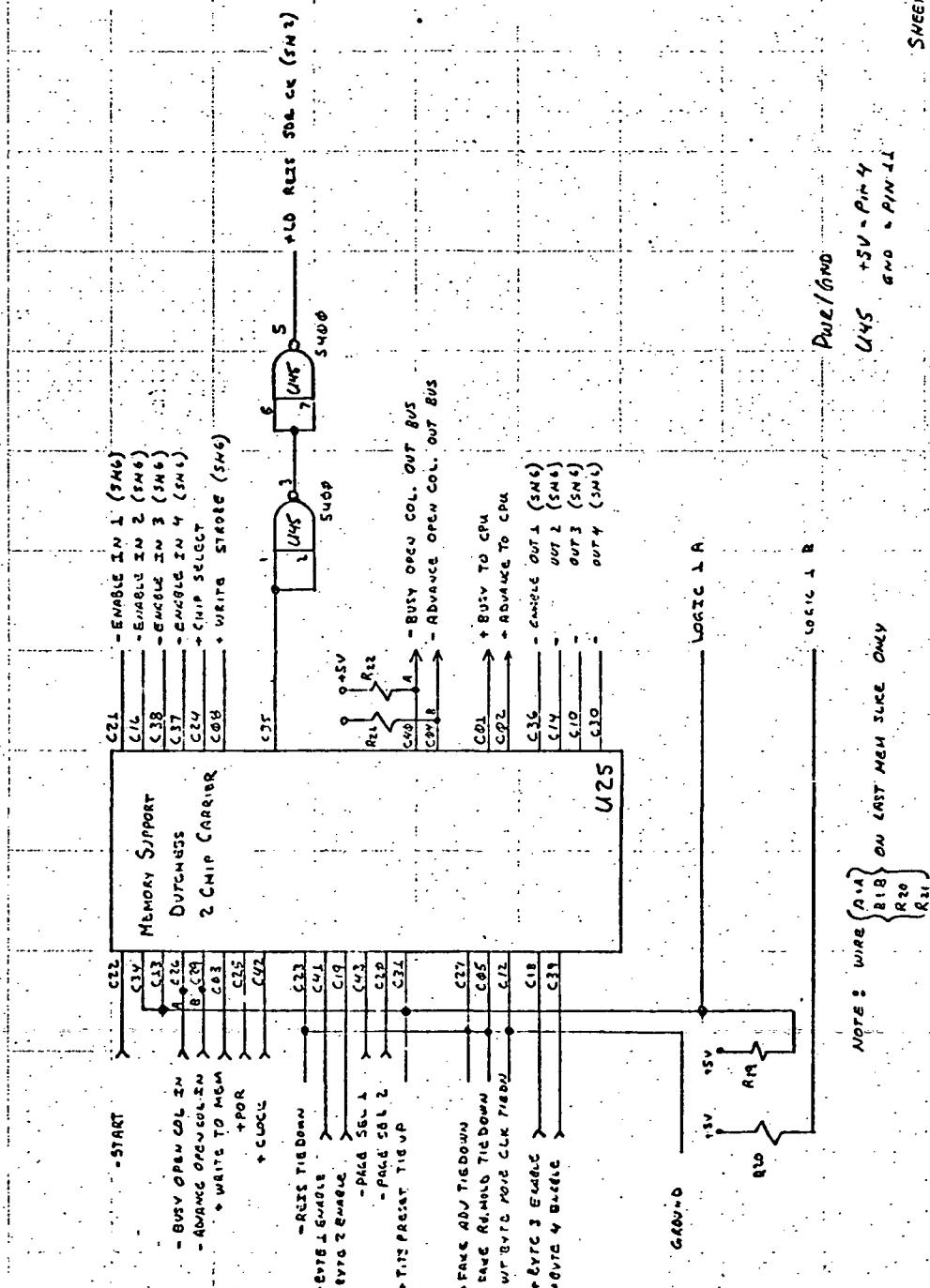
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Power U26 → U43

+8.5V

+V<sub>B</sub>

+3.3V

+V<sub>L</sub>

+V<sub>DD</sub>

+5V

+V<sub>DD</sub>

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-0.8V

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